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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,654	09/18/2003	David Jia Chen	ROC920030233US1	8565

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EXAMINER
NGUYEN, LINH M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,654	CHEN ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-14 are presented in the instant application according to the Applicants' filing on 09/18/2003.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections/Minor Informalities

2. Claim 8 is objected to because of the following informalities:

Line 1, change "claim2" to -- claim 2--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1, 9 and 10, the recitation "a series of at least one stage" renders the claim indefinite since the term "series" means at least two elements are included; thus there should be at least two stages of delay and not just one delay stage as recited. Clarification is required.

With respect to claim 1, 9, 10 and 11, the recitation " *wherein a drain of a top transistor in the stack is coupled to a first reference voltage, wherein a source of a bottom transistor in the stack is coupled to a second reference voltage, and wherein a source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage*" renders the claim indefinite since it is not clear how the output signal would be generated or what the output would be when the input signal received is at low state or in other words when all the transistors would be inactivated. Clarification is required.

Claims 2-8 and 12-14 are also rejected under 35 U.S.C. 112, second paragraph because of their dependency on claim 1 and claim 11, respectively.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 3, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. Patent No. 5,157,279).

With respect to claim 1, 9 and 10, as best understood, Lee discloses, in Figure 3, a circuit arrangement comprising a) an input signal [data] to be delayed and b) a series of at least one

delay stage [5,7], wherein each delay stage includes a stack of uniform minimum channel length transistors [5,7], wherein a gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage, wherein a drain of a top transistor in the stack is coupled to a first reference voltage [Vcc], wherein a source of a bottom transistor in the stack is coupled to a second reference voltage [ground], and wherein a source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage [8].

With respect to claim 3, Lee discloses, in Figure 3, that each transistor is an n-channel FET.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,157, 279).

With respect to claim 4, Lee discloses all of the claimed limitations as expressly recited in claim 1 except for each transistor being a p-channel FET. However, Lee suggests in column 1, lines 14-19, that p-channel FETs could be used in lieu of n-channel FETs.

To modify the delay element of Lee by replacing p-channel FETs with n-channel FETs to produce a high performance output signal would have been obvious to one of ordinary skill in

the art at the time of the invention since Lee teaches that by doing so would provide high output gain (see col. 1, line 8).

Allowable Subject Matter

9. Claims 2 and 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 11-14 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this office action.

The following is a statement of reasons for the indication of allowable subject matter with the examiner's best interpretation of the claims:

The closest prior art on record does not show or fairly suggest:

- A delay element, in which each stack of transistors includes additional transistors electrically coupled with the top transistor and the bottom transistor; wherein a drain of a first additional transistor is electrically coupled to a source of the top transistor, a source of the last additional transistor is connected to a drain of the bottom transistor, and wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack, as called for in claim 2;

- A delay element, in which the input signal to be delayed is a clock signal, as called for in claim 7; and

- A delay circuit having a totem pole of at least two transistors, the totem pole including a top transistor with a drain electrically coupled to a source of the first transistor, a bottom

transistor with a source electrically coupled to a drain of the last transistor, in combination with the remaining claimed limitations, as called for in claim 11.

Citation of Relevant Prior Art

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Sato et al. (U.S. Patent No. 5,602,798) discloses a synchronous semiconductor memory device operable in snooze mode.

Prior art Matsuzaki et al. (U.S. Patent No. 5,302,871) discloses a delay circuit including a first MOS transistor series and a second MOS transistor series.

Prior art Fujii et al. (U.S. Patent No. 4,700,089) discloses a delay circuit for gate-array LSI.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER